

**In the Claims:**

**Claim 1 (previously presented):** A VLIW processor comprising:

first and second register file banks, said first register file bank comprising a first plurality of read ports and write ports, and said second register file bank comprising a second plurality of read ports and write ports;

first and second data path blocks, said first data path block comprising a first plurality of execution units, and said second data path block comprising a second plurality of execution units;

a first plurality of buses coupling said first plurality of read ports to each of said first and second data path blocks;

a second plurality of buses coupling said second plurality of read ports to each of said first and second data path blocks;

wherein an operand residing in said first plurality of read ports is concurrently accessed by said first plurality of execution units in said first data path block and by said second plurality of execution units in said second data path block and wherein a result of an operation performed in said first data path block is written to only said first plurality of write ports without being written to said second plurality of write ports, wherein said VLIW processor does not include a move bus.

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**Claim 2 (original):** The VLIW processor of claim 1 wherein an operand residing in said second plurality of read ports is concurrently accessed by said first plurality of execution units in said first data path block and by said second plurality of execution units in said second data path block.

**Claim 3 (original):** The VLIW processor of claim 1 wherein each of said first and second plurality of execution units is selected from the group consisting of an ALU and a multiplier.

**Claims 4-5 (cancelled).**

**Claim 6 (currently amended):** The VLIW processor of ~~claim 4~~ claim 1 wherein a result of an operation performed in said second data path block is accessed only by said second plurality of write ports without being accessed by said first plurality of write ports.

**Claim 7 (previously presented):** A VLIW processor comprising:  
a plurality of register file banks, each of said plurality of register file banks comprising a respective plurality of read ports and write ports;  
a plurality of data path blocks, each of said plurality of data path blocks comprising a respective plurality of execution units;

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a plurality of buses coupling said plurality of register file banks to each of said plurality of data path blocks;

wherein an operand residing in each of said respective plurality of read ports is concurrently accessed by each of said respective plurality of execution units and wherein a result of an operation performed in one of said plurality of data path blocks is written to only said respective plurality of write ports, wherein said VLIW processor does not include a move bus.

**Claim 8 (original):** The VLIW processor of claim 7 wherein each of said respective plurality of execution units is selected from the group consisting of an ALU and a multiplier.

**Claim 9-10 (cancelled).**

**Claim 11 (previously presented):** A VLIW processor comprising:

first and second register file banks, said first register file bank comprising a first plurality of read ports and write ports, and said second register file bank comprising a second plurality of read ports and write ports;

first and second data path blocks, said first data path block comprising a first plurality of execution units, and said second data path block comprising a second plurality of execution units;

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a first plurality of buses coupling said first plurality of read ports to each of said first and second data path blocks;

a second plurality of buses coupling said second plurality of read ports to each of said first and second data path blocks;

wherein during a single clock cycle an operand residing in one of said first plurality of read ports is accessed by only one of said first plurality of execution units in said first data path block and wherein a result of an operation performed in said first data path block is written to only said first plurality of write ports without being written to said second plurality of write ports, wherein said VLIW processor does not include a move bus.

**Claim 12 (original):** The VLIW processor of claim 11 wherein during said single clock cycle an operand residing in one of said first plurality of read ports is accessed by only one of said second plurality of execution units in said second data path block.

**Claim 13 (original):** The VLIW processor of claim 11 wherein during said single clock cycle an operand residing in one of said second plurality of read ports is accessed by only one of said first plurality of execution units in said first data path block.

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**Claim 14 (original):** The VLIW processor of claim 11 wherein during said single clock cycle an operand residing in one of said second plurality of read ports is accessed by only one of said second plurality of execution units in said second data path block.

**Claim 15 (original):** The VLIW processor of claim 11 wherein each of said first and second plurality of execution units is selected from the group consisting of an ALU and a multiplier.

**Claims 16-17 (cancelled).**

**Claim 18 (currently amended):** The VLIW processor of ~~claim 16~~ claim 11 wherein a result of an operation performed in said second data path block is accessed only by said second plurality of write ports without being accessed by said first plurality of write ports.

**Claim 19 (previously presented):** A VLIW processor comprising:  
a plurality of register file banks, each of said plurality of register file banks comprising a respective plurality of read ports and write ports;  
a plurality of data path blocks, each of said plurality of data path blocks comprising a respective plurality of execution units;

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a plurality of buses coupling said plurality of register file banks to each of said plurality of data path blocks;

wherein during a single clock cycle an operand residing in one of said respective plurality of read ports is accessed by only one of said respective plurality of execution units and wherein a result of an operation performed in one of said plurality of data path blocks is written only to said respective plurality of write ports, wherein said VLIW processor does not include a move bus.

**Claim 20 (original):** The VLIW processor of claim 19 wherein each of said respective plurality of execution units is selected from the group consisting of an ALU and a multiplier.

**Claim 21-22 (cancelled).**